PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/18/10425

Analog, MEMS & Sensors Group (AMS)

Introduction of a new design for BlueNRG-1 products

WHAT:
Progressing on the activities related to quality continuous improvement, ST is glad to announce a new design for BLUENRG1 family to correct some bugs reported on the product.

Material	Current process	Modified process	Comment
Register Die Id	return 0x111	return 0x113	traceability
BOR operating voltage	down to 2.1V	down to 1.7V	To prevent flash corruption at low voltage
Other modifications		- Fix on SWD interface.	
		-Minor functional fixes on AUXADC.	
		Other minor changes to improve the ST manufacturing FT yield.	
		Modification of datasheet and errata sheet	

WHY:

This change will contribute to improve product functionality and improve robustness.

HOW:

The qualification program consists mainly of comparative electrical characterization.
You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:

The new design will be implemented in April 2019.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect negativelythe electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is also no change in the packing process or in the standard delivery quantities.

Shipments may start earlier with the customer's written agreement.

Evaluation Report

Standard Consumer Grade Qualification

F157 BLUENRG-134

F157 BLUENRG-132

General Information	
Product Line	*F157*
Product Description	Bluetooth Low Energy Wireless Processor
P/N	*BLUENRG-134*
Product Group	*AMG*
Product division	*General purpose analog*
Package	*VFQFPN 5x5x0.9 32L-*
Silicon Process technology	*C090LP+flash*

Locations	
Wafer fab	*TSMC Fab14*
Assembly plant	*SUBCO ATP3, UTAC Thai*
Reliability Lab	*Grenoble GRAL*
Reliability assessment	***Pass***

PRODUCTS LIST

Product line	P/N	Package	Assy Plant
F157	BLUENRG-134 BLUENRG-132	Wafer level CSP VFQFPN 5x5 32L	Subco ATT UTAC Thai

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
ADCS0061692	Reliability Tests and Criteria for Product Qualification

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The Aim of this report is to present characterization trials performed to qualify the design change and remind reliability trials performed on F128 BlueNRG (MSQTR and MSCSP), F174 BlueNRG (232/234) and F157 BlueNRG (132/134) products in order to reach qualification. BlueNRG is a Bluetooth Low Energy Wireless Processor based on ARM Cortex M0 core.

3.2 Conclusion

All trials have been performed with good results on both versions.

F157 BlueNRG-134 and BlueNRG-132 products are qualified.

4 DEVICE CHARACTERISTICS

4.1 Device description

life.augmented

BlueNRG-1

Datasheet

Bluetooth® low energy wireless system-on-chip

Product status link
BlueNRG-1

Features

- Bluetooth low energy single mode system-on-chip compliant with Bluetooth specifications:
  - master, slave and multiple simultaneous roles
- Operating supply voltage: from 1.7 to 3.6 V
- Integrated linear regulator and DC-DC step-down converter
- Operating temperature range: -40 °C to 105 °C
- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- Programmable 160 kB Flash
- 24 kB RAM with retention (two 12 kB banks)
- 1 x UART interface
- 1 x SPI interface
- 2 x I²C interface
- 14 or 15 GPIOs
- 2 x multifunction timer
- 10-bit ADC
- Watchdog and RTC
- DMA controller
- PDM stream processor
- 16 or 32 MHz crystal oscillator
- 32 kHz crystal oscillator
- 32 kHz ring oscillator
- Battery voltage and temperature sensors
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- 8.3 mA TX current (@ -2 dBm, 3.0 V)
- Down to 1 µA current consumption with active BLE stack (sleep mode)
- ST companion integrated balun/filter chips are available
- Average advertisement current consumption 15.34 µA (advertisement interval 1000 ms) – 1 year, 8 months, 19 days with 230 mAh battery (CR2032)
- Average connection current consumption 7.059 µA (connection interval 1000 ms) – 3 years, 10 months, 12 days with 230 mAh battery (CR2032)
- Suitable for building applications compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 part 15, ARIB STD-T66
- Pre-programmed bootloader via UART
- QFN32 and WCSP34 package options

Applications

- Watches
- Fitness, wellness and sports

4.2 Construction note

Line:	F128 BLUENRG 1mil	F128 BLUENRG 0.8mil	F128 BLUENRG CSP	F157 BLUENRG-132	F157 BLUENRG-134	F174 BLUENRG-232	F174 BLUENRG-234
Comm. Product:	**BLUENRGQTR**	**BLUENRGQTR**	**BLUENRG CSP**	**BLUENRG-132**	**BLUENRG-134**	**BLUENRG-232**	**BLUENRG-234**
Package Type:	VFQFPN 5.0x5.0x0.9 32L-	VFQFPN 5.0x5.0x0.9 32L-	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4
Die Size:	2600 x 2500 µm	2600 x 2500 µm	2660 x 2560 µm	2710 x 2580 µm	2710 x 2580 µm	2710 x 2580 µm	2710 x 2580 µm
Diffusion Plant:	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14
Assembly Site:	SUBCO ATP3	SUBCO ATP3	SUBCO ATT1	UTAC Thai	SUBCO ATT1	UTAC Thai	SUBCO ATT1
Test Site:	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE
Fab Process:	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash
Passivation:	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE
Die backside:	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon
Die Attach:	Ablestick AMK-6	Ablestick AMK-6	NA	Henkel 8600	NA	Henkel 8600	NA
Mold Compound:	Sumitomo G700	Sumitomo G700	NA	SUMITOMO G700	NA	SUMITOMO G700	NA
Lead Frame:	Copper	Copper	NA	Copper	NA	Copper	NA
Lead Finish:	NiPdAu	NiPdAu	Bump leadfree	Sn	Bump leadfree	Sn	Bump leadfree
Package Size and Pitch:	VFQFPN 5.0x5.0x0.9 32L-Ep0.5	VFQFPN 5.0x5.0x0.9 32L-Ep0.5	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4
Bond Wire:	Gold 1MIL	Gold 0.8MIL	NA	Gold 0.8MIL	NA	Gold 0.8MIL	NA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	QFN32 5x5 1mil	F128	
2	QFN32 5x5 1mil	F128	
3	QFN32 5x5 0.8mil	F128	
4	WLCSP pitch 0.4mm	F128	
5	WLCSP pitch 0.4mm	F128	
6	QFN32 5x5 0.8mil	F157	
7	WLCSP pitch 0.4mm	F174	
8	QFN32 5x5 0.8mil	F174	

Detailed results in below chapter will refer to Lot #.

5.2 Test plan and results summary

Yield verification

Yield on the new design measured in line with ST standard.

Statistical report

	EWS	Final test	Comment
WLCSP (Cpk>1.33)	100%	99.1%	Conform

Reliability

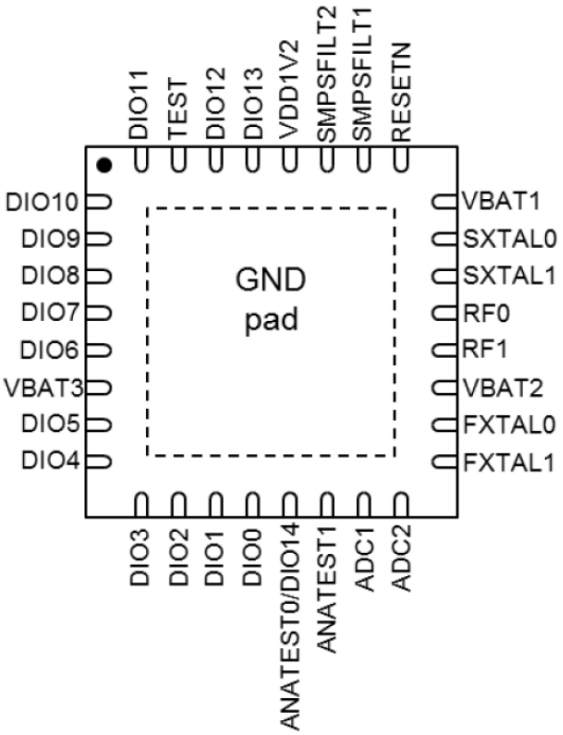
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS								Note
						Lot 1	Lot 2	Lot 3	Lot4	Lot5	Lot6	Lot7	Lot8	
Die Oriented Tests														
HTOL	N	JESD22 A-108	Tj = 125°C, BIAS		168H	0/74	0/78	0/73			0/95			
					500H	0/73	0/78	0/73			0/95			
					1000H	0/73	0/78	0/73						
HTSL	N	JESD22 A-103	Ta = 150°C		168H	0/80	-	-	0/78	0/78	-			
					500H	0/80	-	-	0/78	0/78	-			
					1000H	0/80	-	-	0/78	0/78	-			
ELFR	N	JESD74	Tj = 125°C, BIAS			-	-	0/480	0/239		-			
Package Oriented Tests														
PC		JESD22 A-113	MSL3: Bake 24H @ 125°C Soak 192H @ Ta=30°C RH=60% Oven Reflow @ Tpeak=260°C, 3 times		Final	Pass	-	Pass	Pass	Pass	-			
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96H	-	-	*0/80	*0/79	*0/80	-			*UHAST
					168H	0/78	-				-			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy	-	-	0/80	0/70	0/76	-			
					500cy	0/78	-	0/80	0/70	0/76	-			
					1000cy	0/78	-	0/80	0/70	0/76	-			
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168H	0/76	-	-			-			
					500H	0/75	-	-			-			
					1000H	0/75	-	-			-			
Other Tests														
ESD	N	ADCS 0060102 (JESD22-A114)	HBM			±3KV	-	-	Pass	-		2kV	2kV	
		ADCS 0060102 (ANSI/ESD STM5.3.1)	CDM			±1.5KV	-	-	400V			1000V	1000V	
		ADCS 0060102 (JESD22-A115)	MM			±300V	-	-	160V					
LU	N	ADCS 0018695	Current Inj. Overvoltage		±200mA X1.5	Pass	-	-	Pass			Pass	Pass	

6 ANNEXES

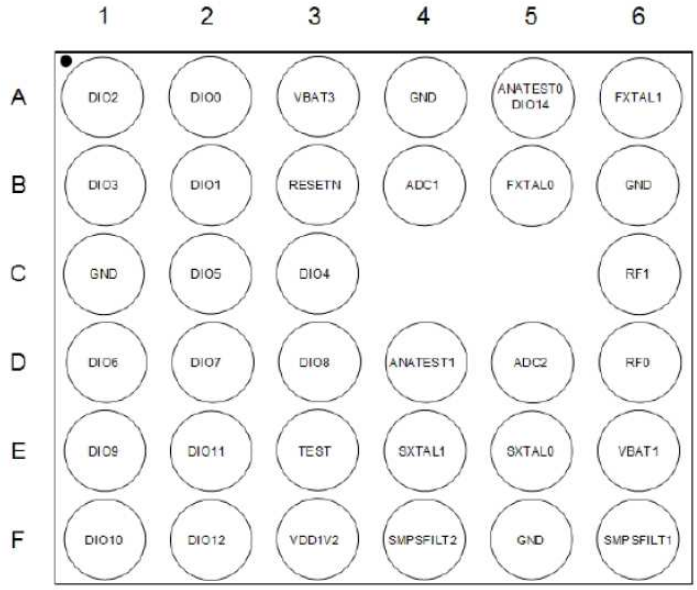
6.1 Device details

6.1.1 Pin connection

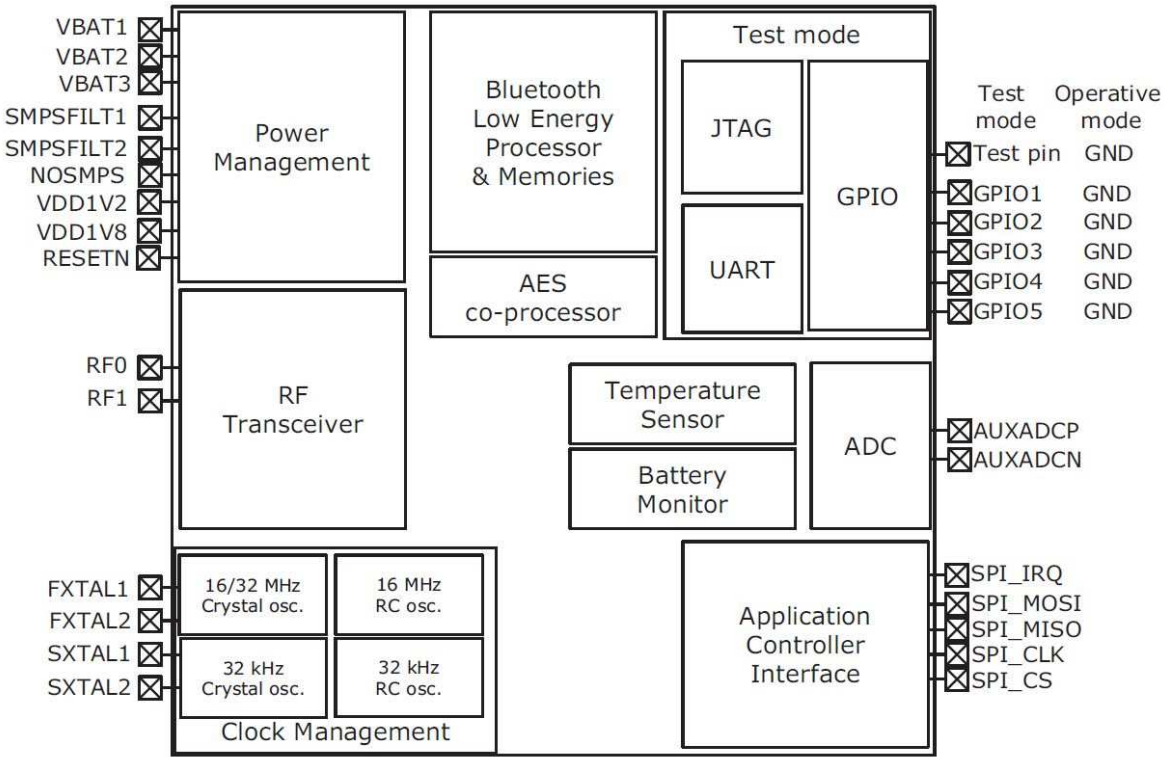
BUENRG-132



BLUENRG-134



Block diagram



6.1.4 Package outline/Mechanical data

TITLE: WLCSP 2.69x2.56x0.5 34 PITCH 0.4 BALL 0.25

PACKAGE CODE: 01C1 (F157)

JEDEC/EIAJ REFERENCE NUMBER: N/A

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A		0.50	0.52		0.50	0.52	
A1	0.16	0.175	0.19	0.16	0.175	0.19	
A2		0.022	0.025		0.022	0.025	
A3	0.285	0.30	0.315	0.285	0.30	0.315	
b		0.27			0.27		(2)
D	2.50	2.56	2.58	2.50	2.56	2.58	(3)
D1		2.00			2.00		
E	2.63	2.69	2.71	2.63	2.69	2.71	(4)
E1		2.00			2.00		
e		0.40			0.40		
f		0.28			0.28		
g		0.35			0.35		
ccc			0.05			0.05	

NOTES:

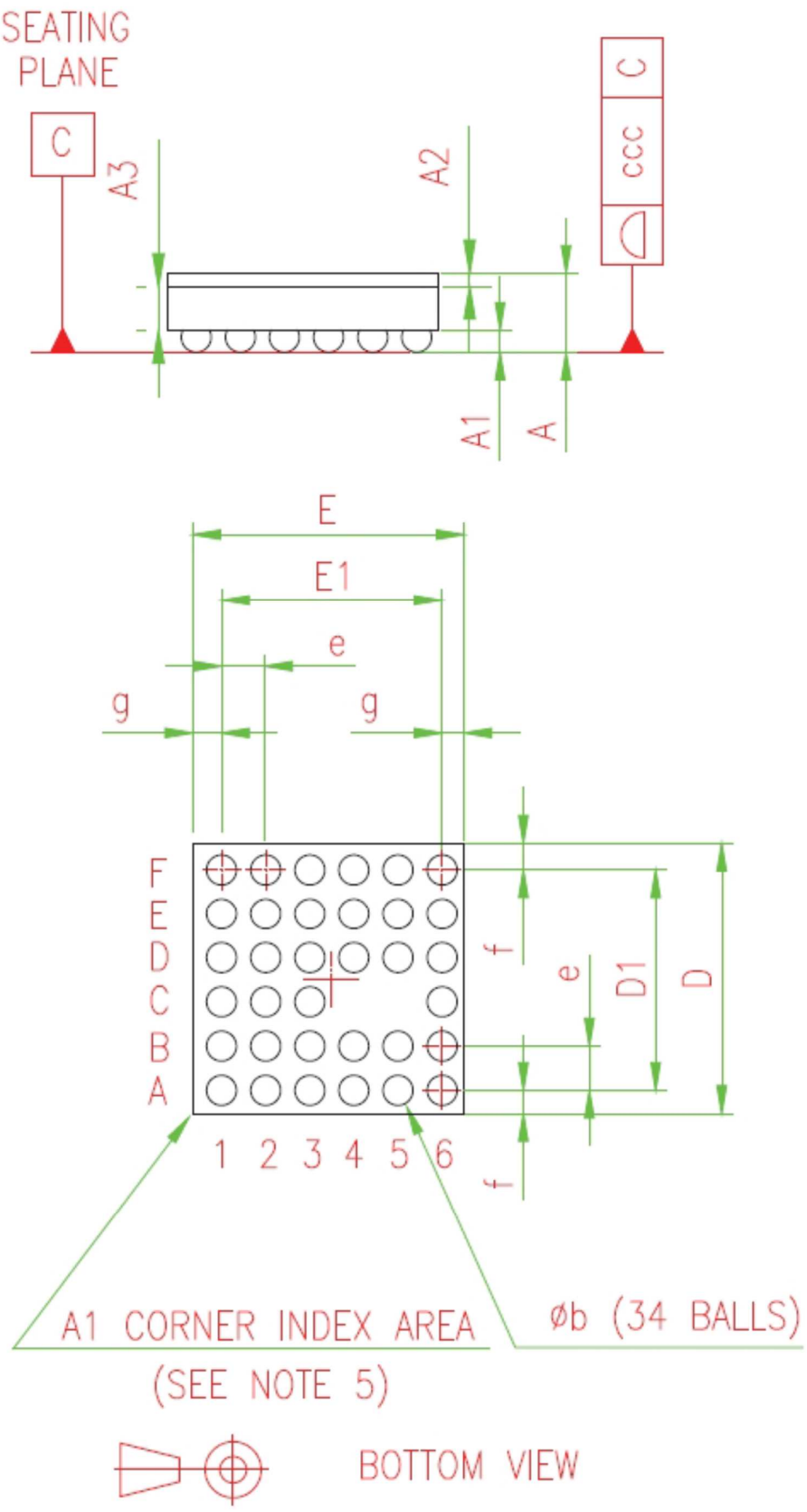
(1) – WLCSP stands for **W**afer **L**evel **C**hip **S**cale **P**ackage.

(2) – The typical ball diameter before mounting is 0.25mm.

(3) – D=f+D1+f.

(4) – E=g+E1+g.

(5) – The terminal A1 corner must be identified on the top surface by using a laser marking dot.


SEATING
PLANE
C
A3
A2
ccc
C
A1
A
E
E1
e
g
g
F
E
D
C
B
A
1 2 3 4 5 6
f
e
D1
D
f
A1 CORNER INDEX AREA
(SEE NOTE 5)
øb (34 BALLS)
BOTTOM VIEW

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.